CLAIMS:

1. A method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers;

(b) receiving one byte of a plurality of N-bit bytes that together define an address in the memory space;

(c) incrementing a count as a result of completing step (b);

(d) addressing one of said two registers according to the incremented count in step (c); and

(e) storing said one byte in the register addressed in step (d).

2. The method of claim 1, further comprising receiving another byte of said plurality of bytes, resetting the count from step (c), addressing the other of said two registers as a result of the reset count, and storing said other byte in said other register.

3. The method of claim 2, further comprising the steps of:

(a) receiving a memory access command; and

(b) accessing the memory space at said address based on said memory access command.

4. The method of claim 3, wherein said memory access command is a write data command.

5. The method of claim 3, wherein said memory access command is a read data command.

6. The method of claim 1, further comprising receiving another byte of said plurality of bytes, incrementing the count from step (c) to obtain a next incremented count, addressing the other of said two registers as a result of the next incremented count, and storing said other byte in said other register.

7. The method of claim 6, further comprising the steps of:

(a) receiving a memory access command; and

(b) accessing the memory space at said address based on said memory access command.

8. The method of claim 7, wherein said memory access command is a write data command.

9. The method of claim 7, wherein said memory access command is a read data command.

10. The method of claim 1, wherein said 2^M address memory space comprises the address space of a memory device.

11. The method of claim 1, wherein said 2^M address memory space comprises the address space of a plurality of memory devices.

12. An apparatus for high speed addressing of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising:

(a) at least two registers;

(b) a counter; and

(c) a logic circuit adapted for:

(i) receiving one byte of a plurality of N-bit bytes that together define an address in the memory space;

(ii) incrementing a count of said counter as a result of completing step (i);

(iii) addressing one of said two registers according to the incremented count in step (ii); and

(iv) storing said one byte in said register addressed in step (iii).

13. The apparatus of claim 12, wherein said logic circuit is further adapted for receiving another byte of said plurality of bytes, resetting the count of said counter, addressing the other of said two registers as a result of the reset count, and storing said other byte in said other register.

14. The apparatus of claim 13, wherein said logic circuit is further adapted for:

(a) receiving a memory access command; and

(b) accessing the memory space at said address based on said memory access command.

15. The apparatus of claim 14, wherein said memory access command is a write data command.

16. The apparatus of claim 14, wherein said memory access command is a read data command.

17. The apparatus of claim 12, wherein said logic circuit is further adapted for receiving another byte of said plurality of bytes, incrementing the count of said counter to obtain a next incremented count, addressing the other of said two registers as a result of the next incremented count, and storing said other byte in said other register.

18. The apparatus of claim 17, wherein said logic circuit is further adapted for:

(a) receiving a memory access command; and

(b) accessing the memory space at said address based on said memory access command.

19. The apparatus of claim 18, wherein said memory access command is a write data command.

20. The apparatus of claim 18, wherein said memory access command is a read data command.

21. The apparatus of claim 12, wherein said 2^M address memory space comprises the address space of a memory device.

22. The apparatus of claim 12, wherein said 2^M address memory space comprises the address space of a plurality of memory devices.

23. A machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, the machine having at least two registers, where M is greater than N, comprising the steps of:

(a) receiving one byte of a plurality of N-bit bytes that together define an address in the memory space;

(b) incrementing a count as a result of completing step (a);

(c) addressing one of the at least two registers according to the incremented count in step (b); and

(d) storing said one byte in the register addressed in step (c).

24. The machine readable medium of claim 23 adapted so that the method further comprises receiving another byte of said plurality of bytes, resetting the count from step (c), addressing the other of said two registers as a result of the reset count, and storing said other byte in said other register.

25. The machine readable medium of claim 24, adapted so that the method further comprises the steps of:

(a) receiving a memory access command; and

(b) accessing the memory space at said address based on said memory access command.

26. The machine readable medium of claim 25, adapted so that wherein said memory access is a write data access.

27. The machine readable medium of claim 25, adapted so that wherein said memory access is a read data access.

28. The machine readable medium of claim 23 adapted so that the method further comprises receiving another byte of said plurality of bytes, incrementing the count from step (c) to obtain a next incremented count, addressing the other of said two

registers as a result of the next incremented count, and then storing said other byte in said other register.

29. The method of claim 28, further comprising the steps of:

(a) receiving a memory access command; and

(b) accessing the memory space at said address based on said memory access command.

30. The machine readable medium of claim 29, adapted so that said memory access is a write data access.

31. The machine readable medium of claim 29, adapted so that said memory access is a read data access.

32. The machine readable medium of claim 23, wherein said 2^M address memory space comprises the address space of a memory device.

33. The machine readable medium of claim 23, wherein said 2^M address memory space comprises the address space of a plurality of memory devices.

34. A method for high speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers, wherein each of said registers contains one of a plurality of N-bit bytes that together define an address in the memory space;

(b) receiving a memory access command; and

(c) accessing the memory space at said address as a result of said memory access command.

35. The method of claim 34, wherein said memory access command is a write data command.

36. The method of claim 34, wherein said memory access command is a read data command.

37. An apparatus for high speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising:

(a) at least two registers, wherein each of said registers contains one of a plurality of N-bit bytes that together define an address in the memory space; and

(b) a logic circuit adapted for receiving a memory access command, and accessing the memory space at said address as a result of said memory access command

38. The apparatus of claim 37, wherein said logic circuit is further adapted so that said memory access is a write data access.

39. The apparatus of claim 37, wherein said logic circuit is further adapted so that said memory access is a read data access.

40. A machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed access of a memory space having 2^M addresses using an N-bit bus, where M is greater than N, comprising the steps of:

(a) providing at least two registers, wherein each of said registers contains one of a plurality of N-bit bytes that together define an address in the memory space;

(b) receiving a memory access command; and

(c) accessing the memory space at said address as a result of said memory access command.

41. The machine readable medium of claim 40, wherein said method is adapted so that said memory access command is a write data command.

42. The machine readable medium of claim 40, wherein said method is adapted so that said memory access command is a read data command.